Fully depleted CCD’s Fabricated on High-Resistivity Silicon

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Fully-depleted CCD technology

Background

- Motivated by SuperNova Cosmology Group
- Spin off of high-energy-physics detector R&D
- Fabrication at LBNL Microsystems Laboratory

Summary of 2k x 2k Results

- Quantum efficiency > 80% at 950 nm
- Excellent charge transfer efficiency (> 0.999995)
- Point spread function Gaussian with $\sigma \sim 10 \, \mu m$ at $V_{sub} = 35V$

Recent Results/In Progress

- Demonstration of $\sim 2$ e- rms noise at 8 $\mu$s sample time
- Demonstration at 800 x 1980 CCD at NOAO KPNO 4m RC spectrometer
- 200 $\mu$m thick CCD PSF measurements at Lick Hamilton Spectrograph
- Preliminary proton irradiation results
- First results at 150 mm wafer foundry (photodiodes)
- Submission of 150 mm wafer CCD layout including test CCD’s for 10 MHz readout, 9 $\mu$m pixel CCD’s, and 4 quadrant readout
Conceived by the LBNL Physics Division to support the detector R&D effort for the Superconducting SuperCollider

Class 10 clean room dedicated to high-purity silicon fabrication

Includes full CCD fabrication capability except ion implantation (3 commercial vendors in the Bay Area)

Equipment includes:

1X lithography for large area CCD development (Intel donation)

Polysilicon and silicon nitride dry etching (partially funded by Keck Telescope Science Steering Committee)

Oxidation and annealing furnaces

Polysilicon, silicon nitride, and silicon dioxide thin film deposition furnaces

Aluminum, silicon dioxide and indium tin oxide deposition (sputtering)

100 mm wafer facility although some equipment can be upgraded to 150 mm

Successful fabrication of 200 x 200, 2048 x 2048, and 2048 x 4096 (15μm)^2 CCD’s
Optical/scanning-electron-microscope photographs taken after poly1 etching
PROPOSAL:
Make a thick CCD on a high-resistivity n-type substrate, operate fully depleted with rear illumination.

Advantages:
1) Conventional MOS processes with no thinning => "inexpensive"
2) Full quantum efficiency to > 1 μm => no fringing
3) Good blue response with suitably designed rear contact
4) No field-free regions for charge diffusion, good PSF

Disadvantages:
1) Enhanced sensitivity to radiation (x-rays, cosmic rays, radioactive decay)
2) More volume for dark current generation
3) Dislocation generation
CCD Technology

Substrate bias voltage depletes substrate ~ independently of clock voltages
CCD Technology

- Conventional CCD fabrication technology with high-resistivity silicon
- Standard processing through the first 8 (of 10) masking steps
- After mask 8 wafers sent out for backgrinding and backside polishing
  — Standard process for thin die applications
- Deposition of thin backside ohmic contact (in-situ doped polysilicon)
  — Back-illuminated photodiode technology licensed to Digirad, Inc for nuclear medical imaging application
- Completion of remaining processing (contact/metal) with 300 μm thick wafer, requiring focus adjustment of lithography equipment at foundry (standard is 500-600 μm)
- Deposition of antireflection coatings on wafer backside

**Successful fabrication of 100 mm front-illuminated control CCD and 150 mm photodiode wafers at commercial foundry**

**LBNL completion of wafers processed through mask 8 by commercial foundry in progress**
Transparent back-side contact technology

Back-illuminated photodiodes

Theoretical maximum without antireflective coating (due to Si reflection)

Quantum efficiency (%) vs. Wavelength (nm)

- 10 nm polysilicon
- 20 nm polysilicon
- 30 nm polysilicon
- 100 nm polysilicon
Transparent back-side contact technology

p-i-n test device on back-illuminated CCD wafer
First large format CCD made at LBNL

2k x 2k, 15 µm pixels.

1980 x 800, 15 µm pixels.
Quantum Efficiency of state-of-the-art CCDs

Image: 200 x 200 15 μm LBNL CCD in Lick Nickel 1m.
Spectrum: 800 x 1980 15 μm LBNL CCD in NOAO KPNO spectrograph.
Instrument at NOAO KPNO 2nd semester 2001 (http://www.noao.edu)
LBNL 2k x 4k

USAF test pattern.

Trap sites found by pocket pumping.

1478 x 4784
10.5 μm

2k x 4k
15 μm

1294 x 4186
12 μm
Amplifier noise studies

“Standard” amplifier connection between floating diffusion and output source follower transistor

Revised version with more aggressive design rules
Sample time is the width of the reset or video integration.
Point Spread Function Issues

Low-resistivity CCD (typically 20 µm thick): PSF dominated by carrier diffusion in field-free regions. \( \sigma = \) Thickness of field-free region.

Calculated CCD potential versus depth

\( V_g - V_{fb} = 10 \text{ V} \)

Channel dose = \( 2 \times 10^{12} \text{ cm}^{-2} \)
Point Spread Function Issues

- Fully depleted CCD: PSF determined by hole transit time in electric field
- For carriers with the same arrival time at the CCD potential wells, the distribution is Gaussian

Constant field approximation

\[
\sigma = \sqrt{2D_p t_{tr}} \quad t_{tr} = \frac{z_{sub}}{v} = \frac{z_{sub}}{\mu_p E} = \frac{z_{sub}^2}{\mu_p (V_{sub} - V_J)}
\]

\[
D_p / \mu_p = kT / q
\]

\[
\sigma = z_{sub} \sqrt{\frac{kT}{q} \left( \frac{2}{V_{sub} - V_J} \right)}
\]

\[
z_{sub} \quad \sim \text{Thickness of CCD}
\]

\[
kT / q \quad \text{Thermal voltage}
\]

\[
V_{sub} - V_J \quad \text{Voltage across drift region}
\]
Hamilton Coude Echelle Spectrograph
FWHM from Calibration Lamp Spectra

All CCDs have 15 μm pixels

<table>
<thead>
<tr>
<th>Device</th>
<th>FWHM (pixels)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loral Frontside</td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>Loral Thinned/Backside</td>
<td>1.90</td>
<td></td>
</tr>
<tr>
<td>LBNL Backside (300 μm)</td>
<td>1.95</td>
<td>40V subr. bias</td>
</tr>
<tr>
<td>LBNL Backside (200 μm)</td>
<td>1.60</td>
<td>40V subr. bias</td>
</tr>
</tbody>
</table>

\[
\sqrt{\frac{1.60^2 - 1.25^2}{1.95^2 - 1.25^2}} \approx 0.67
\]

\[
\sigma \approx \frac{6.4}{9.6} \text{μm}(200/300 \text{μm})_{V_{sub}=40V}
\]

Consistent with pinhole mask/cosmic ray experiments.
Measurement of PSF with pinhole mask

10 V substrate bias

8 µm holes →
2 µm holes →
4 µm holes →
electronics saturation

25 V substrate bias

8 µm holes →
2 µm holes →
4 µm holes →
Measurement of PSF with pinhole mask

Measurements at Lick Observatory
Theoretical MTF calculations

Ideal MTF convolved with 

Normalized spatial frequency

Normalized MTF

- Ideal MTF
- Sigma = (Pixel pitch)/2
- Sigma = (Pixel pitch)/4
- L = (Pixel pitch)/2
- L = (Pixel pitch)/4
Thinned CCD MTF Data

Data from Nordic Optical Telescope
Loral CCD thinned at University of Arizona
Commercialization efforts

- Started with CCD effort on 100 mm wafer processing line
- Front-illuminated high-resistivity CCD’s were successfully produced
- Processing to mask layer 8 at foundry with completion of processing at LBNL in progress (back illuminated)
- Similar effort at the foundry failed due to processing error

- Downsizing of 100 mm line forces change to 150 mm line
- First lot consists of photodiode arrays
  - Simpler process although major high-temperature steps are included
  - Straightforward to test arrays for dark current uniformity
  - First attempt at backgrinding and thinning of 150 mm wafers

- First 150 mm CCD lot will not be thinned for rapid turnaround
  - Lot starts week of March 19th, 9-11 week turnaround

- Second 150 mm lot using same mask set will be processed for back illumination
CCD Technology

CCD fabricated at commercial foundry through mask 8, contact etching and remaining processing performed at LBNL (in progress)

LBNL back end processing no longer viable with switch to 150 mm wafers
150 mm mask layout for 8 x 8 (3 mm x 3 mm pixel) PIN diode arrays.

First wafers delivered late Feb 2001.

Excellent dark current uniformity measured on control wafers. Pixel yield > 98%, 2-3 killer defects per wafer.

First back-illuminated wafers in progress (300, 360 µm).
Dark current measurements on 150 mm wafers

Cloud level is at 0.5 nA/cm²

73172.1-2 at 100V.
(Zero subtracted and area corrected.)

73172.1-8 at 100V.
(Zero subtracted and area corrected.)
Dark current distribution

Pixel current distribution at 100V.

- Number of pixels:
  - $0 < x < 50 \text{ pA}$: 1150, 1183
  - $50 \text{ pA} < x < 100 \text{ pA}$: 44, 22
  - $100 \text{ pA} < x < 500 \text{ pA}$: 8, 7
  - $500 \text{ pA} < x < 100 \text{nA}$: 0, 2
  - $100 \text{nA} < x < 1 \text{ uA}$: 1, 0
  - $> 1 \text{ uA}$: 3, 2
Includes

- 982 x 935 (15 \(\mu m\))^2
- 1230 x 1170 (12 \(\mu m\))^2
- 1402 x 1336 (10.5 \(\mu m\))^2
- 1636 x 1560 (9 \(\mu m\))^2
- 2520^2 (12 \(\mu m\))^2
- 2880^2 (10.5 \(\mu m\))^2
- 2048 x 4096 (15 \(\mu m\))^2
- 512^2 & 1024 x 512 (15 \(\mu m\))^2

Amplifier studies (noise)

- 1200 x 600 (15 \(\mu m\))^2

2-stage amplifiers for high-speed readout
9 μm pixel issues

Poly 2 and 3 overlap of Poly 1 leaves 1 μm gap between Poly 2 and 3. Step coverage concern for misalignment resulting in triple poly overlap.

Channel area only 22.5% of 15 μm pixel due to losses from channel stop (3 μm) and super notch.

Resulting reduced full well could limit readout speed due to lack of fringing fields near full well.

MTF concerns.
Two-stage amplifier studies

Source follower bandwidth

\[ f_{-3db} = \frac{1}{2\pi} \frac{g_m}{C_{load}} \]

Typical design number \( C_{load} \sim 10 \) pF
LBNL standard output transistor \( g_m \sim 150 \) µA/V
Maximum bandwidth \( \sim 2.4 \) MHz

\[ g_m \propto \sqrt{\frac{W}{L} I_{DS}} \]

Keep standard 47/6 1\(^{\text{st}}\) stage transistor for low noise, add 2\(^{\text{nd}}\) stage to drive output. 450/3 output transistor should drive 10 pF at 10MHz with some design margin.
Two-stage amplifier load devices

- Channel-implant resistor
  - Low noise
  - Large temperature coefficient due to temperature dependence of hole mobility
  - JFET-type behavior (pinchoff)
- Poly resistor
  - No high value poly resistor in foundry CCD process
  - Enough room for a gate-poly resistor
  - Requires minimum design rule width, sensitive to process variations
- Transistor
  - Glow concerns for transistor driven deep into saturation
  - Gate and source brought out to pads, separate $V_{dd}$ for each stage
- External resistor
  - Require $< 2.4 \text{ pF}$ for $10\text{MHz}$ operation

All the above implemented on $1200 \times 600$ (15 \text{\mum} pixel) CCD’s as well as on individual amplifier test structures (150 mm wafer layout)
Channel-implant resistor

- 47/6 1\textsuperscript{st} stage transistor
- Channel-implant resistor
- 450/3 output transistor
Channel-resistor temperature dependence

Resistivity vs Temperature

\[ \rho = \rho_0 e^{\frac{E_a}{kT}} \]

- \( \rho_0 \) is the residual resistivity
- \( E_a \) is the activation energy
- \( k \) is the Boltzmann constant
- \( T \) is the temperature

Graph shows the relationship between resistivity and temperature for different sodium concentrations (\( Na \)).
Channel resistor temperature dependence

Sensitivity (ppm/T) vs Temperature

Temperature (K)

Sensitivity (ppm/T)

- Na = 2E16
- Na = 3E16
- Na = 5E16
Transistor load
Gate poly load resistor
External resistor load
Key R&D Issues / Work in Progress

- Commercialization
  - Experience with 300 µm thick, 150 mm diameter wafers
  - Resistivity attainable with 150 mm wafers
    - LBNL 100 mm wafers > 10 kΩ-cm
    - Foundry 150 mm wafers 4.4 – 7.6 kΩ-cm
    - Depletion voltage $\alpha$ (Resistivity)$^{-1}$
- Ground-based astronomy efforts
  - 2048 x 2048 for Hamilton Spectrograph at Lick Observatory (engineering runs)
  - 800 x 1980 for KPNO RC Spectrograph (2001B semester in shared-risk mode)
  - 2048 x 4096 development with Lick CCD Testing Lab for Keck ESI Spectrograph
- Proton irradiations at LBNL 88” Cyclotron
- Collaboration with JPL on $\delta$-doping for back illumination
  - Low temperature process (MBE) done on finished device
  - Does not require foundry processing of thinner than normal wafers
  - Arbitrarily thin for good point spread function
9 \text{\mu m} pixel issues

Multi-amplifier CCD designed at JPL. The serial register is wide for high-speed readout while the pixel size is smaller than in the main array to allow area for the amplifiers.